P22102
128x128 OLED Application Notes
## Revision History

<table>
<thead>
<tr>
<th>Version</th>
<th>Content</th>
</tr>
</thead>
<tbody>
<tr>
<td>X01</td>
<td>First release</td>
</tr>
</tbody>
</table>
DESCRIPTION

P22102 is a 128X128 dot matrix white passive OLED module with controller for many compact portable applications.

FEATURE
- Panel matrix 128x128.
- Driver IC: SSD1327.
- 16 gray scale
- $V_{CC}=15V$
- $V_{CI}=2.6V-3.5V$
- Embedded 128 x 128 x 4 bit SRAM display buffer.
- 8-bit 6800-series Parallel Interface, 8-bit 8080-series Parallel Interface, Serial Peripheral Interface, I²C Interface.
- Screen saving continuous scrolling function in both horizontal and vertical direction.
- Row Re-mapping and Column Re-mapping
- Programmable Frame Rate and Multiplexing Ratio.

FUNCTION BLOCK DIAGRAM
Component:

C1, C2: 4.7uF/35V (Tantalum type) or VISHAY (572D475X0025A2T)
C3, C4: 1uF/16V (0603)
R1: 1M ohm (0603) 1%

This circuit is for 8080 8bits interface.
DC-DC application circuit for OLED module

Recommend components:

The C1: 0.1μF/6.3V.
The C2: 4.7 μF/6.3V.
The C3: 22pF/16V.
The C4: 4.7μF/35V Tantalum type capacitor.
The R1: 1.27M ohm 1%.
The R2: 113K ohm 1%.
The D1: SCHOTTY DIODE.
The L1: 10uH.
The U1: HPA00483DRBR
The R1, R2 and C3 value should be fine tune by customer.

NOTE a. The HPA00483DRBR is low cost DC/DC for TI.
b. The HPA00483DRBR spec. is same as TPS61045.
<table>
<thead>
<tr>
<th>PIN NAME</th>
<th>PIN NO</th>
<th>DESCRIPTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>VSS</td>
<td>1</td>
<td>Ground.</td>
</tr>
<tr>
<td>VCC</td>
<td>2</td>
<td>Power supply for analog circuit.</td>
</tr>
<tr>
<td>VCOMH</td>
<td>3</td>
<td>Com Voltage Output. A capacitor should be connected between this pin and $V_{SS}$.</td>
</tr>
<tr>
<td>GPIO</td>
<td>4</td>
<td>General I/O port.</td>
</tr>
<tr>
<td>VCI</td>
<td>5</td>
<td>Power supply for logic circuit.</td>
</tr>
<tr>
<td>VDD</td>
<td>6</td>
<td>A capacitor should be connected between this pin and $V_{SS}$.</td>
</tr>
<tr>
<td>BS1</td>
<td>7</td>
<td>MCU bus interface selection pins.</td>
</tr>
<tr>
<td>BS2</td>
<td>8</td>
<td>MCU bus interface selection pins.</td>
</tr>
<tr>
<td>VSS</td>
<td>9</td>
<td>Ground.</td>
</tr>
<tr>
<td>IREF</td>
<td>10</td>
<td>Reference current input pin. A resistor should be connected between this pin and $V_{SS}$.</td>
</tr>
<tr>
<td>CS#</td>
<td>11</td>
<td>Chip select input.</td>
</tr>
<tr>
<td>RES#</td>
<td>12</td>
<td>Reset signal input. When it's low, initialization of SSD1327 is executed.</td>
</tr>
<tr>
<td>D/C</td>
<td>13</td>
<td>Data/ Command control. Pull high for write/read display data. Pull low for write command or read status.</td>
</tr>
<tr>
<td>WR#</td>
<td>14</td>
<td>MCU interface input. Data write operation is initiated when it's pull low.</td>
</tr>
<tr>
<td>RD#</td>
<td>15</td>
<td>MCU interface input. Data read operation is initiated when it's pull low.</td>
</tr>
<tr>
<td>D0</td>
<td>16</td>
<td>Data bus(for parallel interface)</td>
</tr>
<tr>
<td>D1</td>
<td>17</td>
<td></td>
</tr>
<tr>
<td>D2</td>
<td>18</td>
<td></td>
</tr>
<tr>
<td>D3</td>
<td>19</td>
<td></td>
</tr>
<tr>
<td>D4</td>
<td>20</td>
<td></td>
</tr>
<tr>
<td>D5</td>
<td>21</td>
<td></td>
</tr>
<tr>
<td>D6</td>
<td>22</td>
<td></td>
</tr>
<tr>
<td>D7</td>
<td>23</td>
<td></td>
</tr>
<tr>
<td>VCC</td>
<td>24</td>
<td>Power supply for analog circuit.</td>
</tr>
<tr>
<td>VSS</td>
<td>25</td>
<td>Ground.</td>
</tr>
</tbody>
</table>
/*128x128 OLED driver program */
void initial(void)
{
    comm_out(0xae);//Set display off
    comm_out(0xa0);//Set re-map
    comm_out(0x43);
    comm_out(0xa1);//Set display start line
    comm_out(0x00);
    comm_out(0xa2);//Set display offset
    comm_out(0x00);
    comm_out(0xa4);//Normal Display
    comm_out(0xa8);//Set multiplex ratio
    comm_out(0x7f);
    comm_out(0xab);//Function Selection A
    comm_out(0x01);//Enable internal VDD regulator
    comm_out(0x81);//Set contrast
    comm_out(0x77);
    comm_out(0xb1);//Set Phase Length
    comm_out(0x31);
    comm_out(0xb3);//Set Front Clock Divider /Oscillator Frequency
    comm_out(0xb1);
    comm_out(0xb4); //For brightness enhancement
    comm_out(0xb5);
    comm_out(0xb6);//Set Second pre-charge Period
    comm_out(0x0d);
comm_out(0xbc);//Set Pre-charge voltage
comm_out(0x07);

comm_out(0xbe);//Set VCOMH
comm_out(0x07);

comm_out(0xd5);//Function Selection B
comm_out(0x02);//Enable second pre-charge

comm_out(0xaf);//Display on
}
After initial the driver IC, user must clear the whole DDRAM.

```c
void cleanDDR(void)
{
    int i,j;
    comm_out(0x15); // Set column address
    comm_out(0x00); // Column Start Address
    comm_out(0x3f); // Column End Address
    comm_out(0x75); // Set row address
    comm_out(0x00); // Row Start Address
    comm_out(0x7f); // Row End Address
    for(i=0;i<128;i++)
    {
        for(j=0;j<64;j++)
        {
            data_out(0x00);
        }
    }
}
```

```c
void show_data(char a)
{
    int i,j;
    comm_out(0x15); // Set column address
    comm_out(0x00); // Column Start Address
    comm_out(0x3f); // Column End Address
    comm_out(0x75); // Set row address
    comm_out(0x00); // Row Start Address
    comm_out(0x7f); // Row End Address
    for(i=0;i<128;i++)
    {
        for(j=0;j<64;j++)
        {
            data_out(a);
        }
    }
}
```
Power ON / OFF Sequence

Power ON sequence:
1. Power ON V_{CI}.
2. After V_{CI} becomes stable, set wait time at least 1ms (t_0) for internal V_{DD} become stable. Then set RES# pin LOW (logic low) for at least 100us (t_1) \(^{(4)}\) and then HIGH (logic high).
3. After set RES# pin LOW (logic low), wait for at least 100us (t_2). Then Power ON V_{CC} \(^{(1)}\)
4. After V_{CC} become stable, send command AFh for display ON. SEG/COM will be ON after 200ms(t_{AF}).

### The Power ON sequence.

<table>
<thead>
<tr>
<th>V_{CI}</th>
<th>OFF</th>
<th>RES#</th>
<th>GND</th>
<th>V_{CC}</th>
<th>OFF</th>
<th>SEG/COM</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>ON</td>
</tr>
</tbody>
</table>

\[\begin{align*}
\text{V}_{\text{CI}} & \quad \text{OFF} \quad \text{RES#} \quad \text{GND} \quad \text{V}_{\text{CC}} \quad \text{OFF} \quad \text{SEG/COM} \\
\text{ON} & \quad \text{V}_{\text{DDO}} \quad \text{Send AFh command for Display ON} \\
\end{align*}\]

### Power OFF sequence:
1. Send command AEh for display OFF.
2. Power OFF V_{CC} \(^{(1)}\), \(^{(2)}\), \(^{(3)}\)
3. Wait for t_{OFF}. Power OFF V_{CI} (where Minimum t_{OFF}=80ms \(^{(5)}\), Typical t_{OFF}=100ms)

### The Power OFF sequence.

\[\begin{align*}
\text{Send command AEh for display OFF} \quad \text{OFF V}_{\text{CC}} \quad \text{OFF V}_{\text{CI}} \quad \text{V}_{\text{DDO}} \\
\text{V}_{\text{CC}} & \quad \text{OFF} \quad \text{OFF V}_{\text{CC}} \quad \text{OFF} \quad \text{OFF} \\
\end{align*}\]

**Note:**
(1) Since an ESD protection circuit is connected between V_{CI} and V_{CC}, V_{CC} becomes lower than V_{CI} whenever V_{CI} is ON and V_{CC} is OFF as shown in the dotted line of V_{CC} in above figures.
(2) V_{CC} should be kept disable when it is OFF.
(3) Power pins (V_{CI}, V_{CC}) can never be pulled to ground under any circumstance.
(4) The register values are reset after t_1.
(5) V_{CI} should not be Power OFF before V_{CC} Power OFF.
Graphic Display Data RAM Address Map

The GDDRAM is a bit mapped static RAM holding the bit pattern to be displayed. The size of the RAM is 128x128x4 bits. For mechanical flexibility, re-mapping on both Segment and Common outputs can be selected by software. The GDDRAM address maps below tables show some examples on using the command “Set Re-map” A0h to re-map the GDDRAM. In the following tables, the lower nibble and higher nibble of D0, D1, D2 … D8191, D8190, D8191 represent the 128x128 data bytes in the GDDRAM.

The GDDRAM map under the following condition:

- Command “Set Re-map” A0h is set to:
  - Disable Column Address Re-map (A[0]=0)
  - Disable Nibble Re-map (A[1]=0)
  - Enable Horizontal Address Increment (A[2]=0)

- Display Start Line=00h

- Data byte sequence: D0, D1, D2 … D8191

<table>
<thead>
<tr>
<th>Command</th>
<th>Column Address</th>
<th>Column Address (HEX)</th>
</tr>
</thead>
<tbody>
<tr>
<td>COM0</td>
<td>00</td>
<td>3E</td>
</tr>
<tr>
<td>COM1</td>
<td>01</td>
<td>3E</td>
</tr>
<tr>
<td>COM126</td>
<td>7E</td>
<td>8E</td>
</tr>
<tr>
<td>COM127</td>
<td>7F</td>
<td>8F</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Row Address (HEX)</th>
<th>SEG Outputs</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>SEG0 SEG1 SEG2 SEG3 SEG12 SEG125 SEG126 SEG127</td>
</tr>
<tr>
<td></td>
<td>00 01 3E 3F</td>
</tr>
</tbody>
</table>

Nibble re-map A[1]=0
The GDDRAM map under the following condition:

- Command “Set Re-map” A0h is set to:
  - Disable Column Address Re-map (A[0]=0)
  - Disable Nibble Re-map (A[1]=0)

- Display Start Line=00h
- Data byte sequence: D0, D1, D2 ... D8191

GDDRAM address map 2

<table>
<thead>
<tr>
<th>SEG0</th>
<th>SEG1</th>
<th>SEG2</th>
<th>SEG3</th>
<th>SEG12C</th>
<th>SEG12D</th>
<th>SEG12E</th>
<th>SEG12F</th>
<th>SEG127</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Display Start Line=00h
Data byte sequence: D0, D1, D2 ... D8191

The GDDRAM map under the following condition:

- Command “Set Re-map” A0h is set to:
  - Enable Column Address Re-map (A[0]=1)
  - Enable Horizontal Address Increment (A[2]=0)

- Display Start Line=00h
- Data byte sequence: D0, D1, D2 ... D8191

GDDRAM address map 3

<table>
<thead>
<tr>
<th>SEG0</th>
<th>SEG1</th>
<th>SEG2</th>
<th>SEG3</th>
<th>SEG12C</th>
<th>SEG12D</th>
<th>SEG12E</th>
<th>SEG12F</th>
<th>SEG127</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Display Start Line=00h
Data byte sequence: D0, D1, D2 ... D8191

GDDRAM address map 2
The example in which the display start line register is set to 10h with the following condition:

- Command “Set Re-map” A0h is set to:
  - Disable Column Address Re-map (A[0]=0)
  - Disable Nibble Re-map (A[1]=0)
  - Enable Horizontal Address Increment (A[2]=0)
- Display Start Line=78h (corresponds to COM119)
- Data byte sequence: D0, D1, D2 ... D8191

The GDDRAM map under the following condition:

- Command “Set Re-map” A0h is set to:
  - Disable Column Address Re-map (A[0]=0)
  - Disable Nibble Re-map (A[1]=0)
  - Enable Horizontal Address Increment (A[2]=0)
- Display Start Line=00h
- Column Start Address=01h
- Column End Address=3Eh
- Row Start Address=01h
- Row End Address=7Eh
- Data byte sequence: D0, D1, D2 ... D7811
Thank You